IN THE CLAIMS

Please amend claims 1, 3 and 5-9 as shown below. A clean version of the entire set of pending claims 1-9 follows per 37 CFR § 1.121(c)(3). A marked-up copy of claims 1, 3, and 5-9, showing all changes made relative to the previous version of the claim(s), accompanies this paper on separate sheets.

A1

1. (AMENDED) A processor that is configured to execute program instructions that are stored in a memory, said processor comprising:

a default-register that is configured to contain a default-destination-address; and

wherein the program instructions include:

a first instruction that is configured to cause the processor to concurrently load a specified address into the default-register to form the default-destination-address and execute program instructions that are located in the memory at the default-destination-address contained in the default-register, and

a second instruction that is configured to cause the processor to subsequently execute the program instructions that are located in the memory at the default-destination-address contained in the default-register.

2. The processor of claim 1,

wherein the second instruction includes a condition test and is further configured to cause the processor to execute program instructions that are located at the default-destination-address independence upon a result of the condition test.

3. (AMENDED) The processor of claim 1,

wherein the default-register is further configured to contain a default-condition-test; and

wherein the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the default-condition-test contained in the default-register.

4. The processor of claim 1,

wherein the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of a prior condition-test.

5. (AMENDED) The processor of claim 1,

wherein the default-register is further configured to contain a default-condition-test; and

wherein the program instructions further include:

a third instruction that is configured to cause the processor to execute program instructions that are located at another specified address in dependence upon a result of the default-condition-test contained in the default-register.

6. (AMENDED) A processor that is configured to execute program instructions that are stored in a memory, said processor comprising:

a default-register that is configured to contain a default-condition-test; and

wherein the program instructions include:

a first instruction that is configured to cause the processor to concurrently load a specified condition into the default-register to form the default-condition-test and execute program instructions that are located in the memory at a destination-address based on a result of the default-condition-test, and

a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at a destination-address based on a result of the default-condition-test.

A1

7. (AMENDED) A method of controlling a sequence of program instructions, said method comprising:

executing a first instruction that concurrently specifies a destination-address and conditionally causes the default-destination address to become a next instruction address during a first processing cycle;

subsequent to an execution of the first instruction, executing a second instruction that causes the default-destination-address to become the next instruction address during a second processing cycle; and

subsequent to an execution of the second instruction, executing a third instruction that is located at the next instruction address.

8. (AMENDED) The method of claim 7, further comprising:

executing a fourth instruction, before executing the second instruction, that specifies a condition-test; and

wherein causing the default-destination-address to become the next instruction address during the second processing cycle is dependent upon a result of the condition-test when the second instruction is executed.

9. (AMENDED) The method of claim 7, further comprising:

saving a result of a condition-test, before executing the second instruction; and

wherein causing the default-destination-address to become the next instruction address during the second processing cycle when executing the second instruction is dependent upon the result of the condition-test.